REMARKS

This is intended as a full and complete response to the Final Office Action dated September 30, 2004, having a shortened statutory period for response set to expire on December 30, 2004. Claims 1-22 and 24 are pending in the application. Claim 23 has been cancelled. Applicants submit this response to place the application in condition for allowance or in better form for appeal. Please reconsider the claims pending in the application for reasons discussed below.

Claim Rejections - 35 USC § 102

Claims 14, 17, 18 and 19-24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by *Benkeser et al.* (US 5,361,362, hereinafter *Benkeser*). Applicants traverse this rejection as follows.

Applicants submit that each of these claims contains elements directed to updating timestamp values. While the timestamp values are stored in memory locations specified by a processor (or firmware running on a processor), operations for updating the timestamp values and storing them to the specified memory locations are performed without processor interaction. Applicants submit that *Benkeser* does not teach such autonomous timestamp updating, as claimed.

In contrast, Applicants submit that the only timestamp updating taught in *Benkeser* are performed by a processor. In the Office Action, the Examiner refers to portions of *Benkeser* that describe a hardware timer circuit and a holding time field. Applicants submit, however, that the only type of elapsed time calculations and updating of this holding time field taught by *Benkeser* involve processor interaction. Specifically, *Benkeser* teaches that operations for updating the holding time field, which are illustrated in FIG. 4, are performed by a processor (see col. 6, lines 45-47).

Thus, *Benkeser* does not teach that the updating of the timestamp is conducted autonomously from any central processing unit or complex processor system, as claimed. Accordingly, Applicants submit that the claims are patentable over *Benkeser* and respectfully request withdrawal of the rejection.

Claim Rejections - 35 USC § 103

Claims 1, 2, 6 and 7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Benkeser* in view of *Hurvig et al.* (US 6,507,592, hereinafter *Hurvig*).

Claim 1 also contains elements directed to updating timestamp values autonomously by hardware, without processor intervention. For reasons discussed above, Applicants submit that *Benkeser* does not teach these elements, as claimed. The Examiner only relies on *Hurvig* as teaching recording timestamps in firmware. Because *Hurvig* does not teach or suggest any of the claimed elements not taught by *Benkeser*, Applicants submit that, even in combination, these references fail to teach the elements, as claimed.

Accordingly, Applicants submit that claim 1 is patentable over *Benkeser* and *Hurvig*. Claims 2, 6, and 7 each depend from claim 1 and, therefore, each contain the same limiting features as independent claim 1. Accordingly, Applicants submit that claims 2, 6, and 7 are each patentable over *Benkeser* and *Hurvig*, and request withdrawal of this rejection.

Claims 3, 4 and 8-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Benkeser* in view of *Hurvig* and further in view of *Matsuzaki* (US 6,253,305).

Claim 8 recites that a contents of a location in memory used for storing a timestamp are read back and updated with hardware based operations (without firmware interaction). As discussed above, Applicants submit that *Benkeser* and *Hurvig*, even taken together, do not teach these elements, as claimed. The Examiner relies *Matsuzaki* as teaching reading the contents of a register, adding a value to these contents and writing this result to a location indicated by an address. Because *Matsuzaki* does not teach or suggest any of the claimed elements not taught by the combination of *Benkeser* and *Hurvig*, Applicants submit that, even in combination, these references fail to teach the elements, as claimed.

Thus, Applicants submit that claim 8 is patentable over *Benkeser, Hurvig*, and *Matsuzaki*. Applicants further submit that claim 1 is patentable over *Benkeser, Hurvig*, and *Matsuzaki* for similar reasons. Claims 3 and 4 each depend from claim 1 and, therefore, each contain the same limiting features as independent claim 1. Accordingly,

Applicants submit that claims 3 and 4 are each patentable over *Benkeser, Hurvig*, and *Matsuzaki*, and request withdrawal of this rejection.

Claim 5 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Benkeser et al.* in view of *Hurvig et al.* as applied to claim 1 above, and further in view of *Bhatt et al.* (US 4,636,967, hereinafter *Bhatt*).

Claim 5 is dependent from claim 1 which, Applicants submit is patentable over *Hurvig* and *Benkeser* for reasons explained above. Applicants also submit that the teachings of *Bhatt* do not affect the patentability of claim 1. Therefore, as claim 5 is dependent from claim 1, and contains all the limiting features thereof, Applicants also submit that claim 5 is patentable over *Hurvig, Benkeser,* and *Bhatt* and respectfully request withdrawal of this rejection.

Claims 15 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Benkeser et al.*, as applied to claim 14 above, in view of *Matsuzaki et al.*

Claims 15 and 16 are dependent from claim 14 which, Applicants submit is patentable over *Benkeser* for reasons explained above. Applicants also submit that the teachings of *Matsuzaki* do not affect the patentability of claim 14. Therefore, as claims 15 and 16 are dependent from claim 14, and contain all the limiting features thereof, Applicants also submit that claims 15 and 16 are patentable over *Benkeser,* and *Matsuzaki* and respectfully request withdrawal of this rejection.

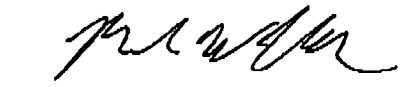
Examiner's Response to Arguments

While the Examiner refers to a hardware timer circuit disclosed in *Benkeser*, the Examiner fails to indicate how this hardware timer circuit is used to update, without processor intervention, a memory location with timestamp information. In contrast, as described above, Applicants submit that the only mention of updating timestamp information in *Benkeser* describes operations (shown in FIG. 4) *performed by a processor* for adding a value from the timer circuit to a holding field.

CONCLUSION

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,



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